Stability under Gate Bias Stressing of Amorphous Oxide Thin Film Transistors

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Stability of amorphous zinc tin oxide thin film transistors (TFTs) is investigated under positive bias stressing (PBS) at temperatures between 65 and 105 °C. The time and temperature dependence of the threshold voltage shift is analyzed using a thermalization energy concept. A maximum energy barrier to defect migration of 0.76 eV and the attempt-to-escape frequency of 10^7 s^{-1} are extracted. These values are compared with those under PBS of amorphous indium gallium zinc oxide and hydrogenated amorphous silicon TFTs. The oxygen vacancy migration model that was proposed for amorphous oxide semiconductors is contrasted with the defect creation model that was proposed for amorphous silicon.

Introduction

Amorphous oxide semiconductors (AOS) are highly transparent, wide band gap materials with high carrier mobility (≥ 10 cm^2 V^{-1} s^{-1}) which are suitable for channel layers in thin film transistors (TFTs) (1). They can be produced with good uniformity, reproducibility and scalability as required by display industries (2). Moreover, the AOS can be deposited at plastic-compatible processing temperatures (< 150 °C) and this has extended their application in many new areas such as flexible and wearable electronics (3). With the emergence of AOS as the leading alternative to hydrogenated amorphous silicon (a-Si:H) for displays and large area electronics, understanding of the stability of these devices becomes vitally important.

Instabilities in amorphous semiconductors are due to the presence of defect states within the bandgap originating from structural disorder (4). In covelantly-bonded a-Si:H, the disorder leads to the presence of silicon dangling bonds and weak Si—Si bonds. The width of the conduction band tail is ~ 30 meV and the density of states (DOS) at the mobility edge is ~ 5×10^{21} cm^{-3} (5). Such a high density of tail states means that the Fermi level is not able to move into the extended states. Therefore, extended state conduction is very limited in a-Si:H and carrier transport is dominated by hopping between localized tail-states. In the AOS, one consequence of disorder is oxygen vacancies which are formed during material depositions. Compare to a-Si:H, AOSs have a narrower width of the conduction band tail (~ 20 meV) and much lower DOS at the mobility edge (~ 10^{18} cm^{-3}). This allows the Fermi level to rise through fewer trap states to reach the mobility edge, leading to a much sharper TFT turn-on characteristic in AOS TFTs (5).

Experimental investigations of the instability in a-Si:H TFTs can be categorized into either light-induced or bias-induced experiments. The threshold voltage (V_{th}) shift was observed in a-Si:H TFTs after prolong illumination, which is known as the Staebler-Wronski effect (6). This metastable effect is attributed to the breaking of weak Si—Si bonds due to the occupation of antibonding states (7). This is a limiting factor to the application of a-Si:H in solar cells and active-matrix displays. In AOS, simple bond breaking does not occur due to their ionic bonding (5). In spite of that, AOS TFTs still suffer from instability. Various experiments such as illumination (8-10), gate or drain bias stressing (11-13), and constant current stressing (14) have been reported. Most investigations focus on the leading AOS material, amorphous indium gallium zinc oxide (a-IGZO), but also on other materials such as amorphous zinc tin oxide (a-ZTO), indium zinc oxide and polycrystalline zinc oxide (15-17). Moreover, the deposition technology, choice of gate dielectric, use of passivation layers and operation environment can also affect the device stability, as previously reported in a comprehensive review by Conley (18).

In this work, we focus on gate bias stressing – namely positive bias stress (PBS) and negative bias illumination stress (NBIS). It has been widely reported that AOS TFTs exhibited a positive threshold voltage (V_{th}) shift under PBS and a negative V_{th} under NBIS. The rate of the V_{th} shift is strongly temperature-dependent in the range from room temperature up to ~ 120 °C when structural changes are not happening (19). The V_{th} shift can be unified for different stressing times and temperatures using the thermalization energy concept (20). A material is assumed as having a number of sites with the potential to suffer some change which would lead to a threshold voltage shift. Thus, a material in its equilibrium can be described as having a distribution of energy barriers to this change process, $D(E)$. If the equilibrium is disturbed (for example, application of a gate bias) at a time $t = 0$, then to a first order approximation after a time t at a temperature T, all potential sites with an energy barrier less than or equal to a thermaliation energy, E_{th}, will suffer a change. Therefore,

$$E_{th} = k_B T \ln(\nu t) \qquad [1]$$

where k_B is the Boltzmann constant and ν is the attempt-to-escape frequency. Equation [1] allows $D(E)$ to be determined. The peak energy barrier to defect conversion, E_{max}, and ν are extracted. The thermalization energy analysis was widely used for various types of silicon thin film silicon TFTs (20-22).

In a recent paper, we have investigated the stability of a-IGZO TFTs under PBS and applied the thermalization energy analysis to explain the V_{th} shift observed (23). In this paper, we extend our study to a-ZTO TFTs. The extracted parameters from the thermalization energy analysis for a-ZTO TFTs are compared with those of a-IGZO TFTs and thin film silicon TFTs. Moreover, the oxygen vacancy migration model that was proposed for AOS is contrasted with the defect creation model that was proposed for amorphous silicon.

Experimental Details

Staggered bottom gate architecture TFTs are produced employing a-ZTO as the channel layer and thermal SiO_2 as the gate dielectric. Deposition of a-ZTO thin films have been reported elsewhere (24). Thin films ~50 nm thickness were sputtered from zinc:tin alloy target with 10 atomic % tin by remote plasma reactive sputtering using oxygen as the reactive gas. The a-ZTO has a tin composition of ~ 33 atomic %, making the film stoichiometrically close to Zn_2SnO_4. These films are incorporated in TFTs after a post-deposition annealing at 500 °C for 1 hour in air. Highly-doped p-type silicon is used for the substrate and gate electrode and aluminum was thermally evaporated after annealing to form the source and drain electrodes. The a-ZTO channel was not passivated.

TFTs were subjected to a gate bias stress field of 1 MV cm^{-1} over the initial threshold field (E_{th}) and I_{DS} was measured as a function of time up to 80,000 s at temperatures of 65, 85 and 105 °C. The applied field is limited to E_{th} + 1 MV cm^{-1} to minimize charge injection into the dielectric that happens with degradation in sub-threshold slope and mobility (18, 25). Moreover, this is the order of the electric field commonly used in TFTs in displays (19). The detail of the bias stress measurement can be found elsewhere (23). An enclosed probe station with a heating stage which is resistively heated by a low noise dc power supply (HP6642A) was used. Transistor characteristics were measured using an HP4140B dual voltage source picoammeter. Three separate TFTs but with similar channel width to length (W/L) and similar device characteristics are used for PBS for different temperatures. It is also possible to use only one device for all three temperatures, as long as annealing is performed to equilibrate the defects at around 200 °C for 1 hour with no applied biases between runs (23).

Results and Discussion

Figure 1a shows a typical gate transfer characteristic for a-ZTO TFT fabricated using the remote plasma reactive sputtering. The devices have a V_{th} of 6.2 V in the linear regime, a switching ratio of ~10^8, a field effect mobility 13.8 $cm^2\ V^{-1}\ s^{-1}$, and a sub-threshold slope of ~ 1 V dec^{-1}. The drain transfer characteristics in Figure 1b confirms that there is no current crowding at the source and drain contacts.

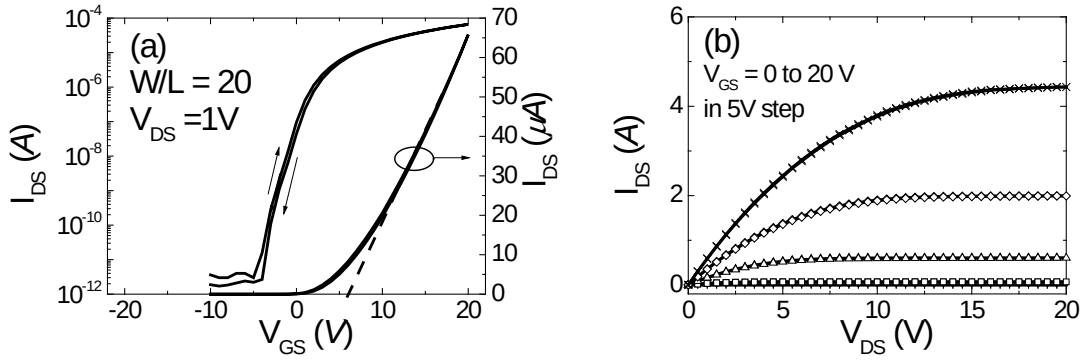

Figure 1. The gate transfer (a) and drain transfer (b) characteristics of a TFT incorporating an a-ZTO channel with a channel width and length of 1000 μm and 50 μm (W/L =20)

Figure 2a shows the linear I_{DS}-V_{GS} graph for a device under PBS at a temperature of 65 °C. The V_{th} is 1.5 V initially and is increased to 10 V after 10,000 s and to 16 V after 50,000 s. The parallel transfer curves above threshold before and after the stress measurements indicate that no degradation of the device occurs due to bias stress (i.e. there is no structural change in the a-ZTO material). As shown in a dashed line in Figure 2a, the increase in V_{th} is linearly related to the decrease in I_{DS} with time. With a gate stress voltage of 1 MV cm^{-1}, Figure 2b shows that the I_{DS} decrease would approach 0 for a stressing time longer than 50,000 s. As expected the rate at which I_{DS} approaches 0 is faster at higher temperatures (~ 40,000 s at 85 °C and ~ 10,000 s at 105 °C) which are also shown. Figure 2c shows the normalized threshold voltage shift, $\Delta V_{thn}(t)$, as a function of gate bias stressing time. $\Delta V_{thn}(t)$ is defined by

$$\Delta V_{thn}(t) = \frac{V_{th}(t) - V_{th}(0)}{V_{th}(\infty) - V_{th}(0)} \qquad [2]$$

where $V_{th}(t)$ is the threshold voltage after some stressing time t, $V_{th}(0)$ is the threshold voltage at 0 s and $V_{th}(\infty)$ is the value to which the threshold voltage is tending after a long stressing time. Significantly, it should be noted that our bias stress program allows us to continuously monitor I_{DS}, and thus V_{th}, continuously, whereas only a few data points for the whole stressing time is generally reported by other groups (13, 16).

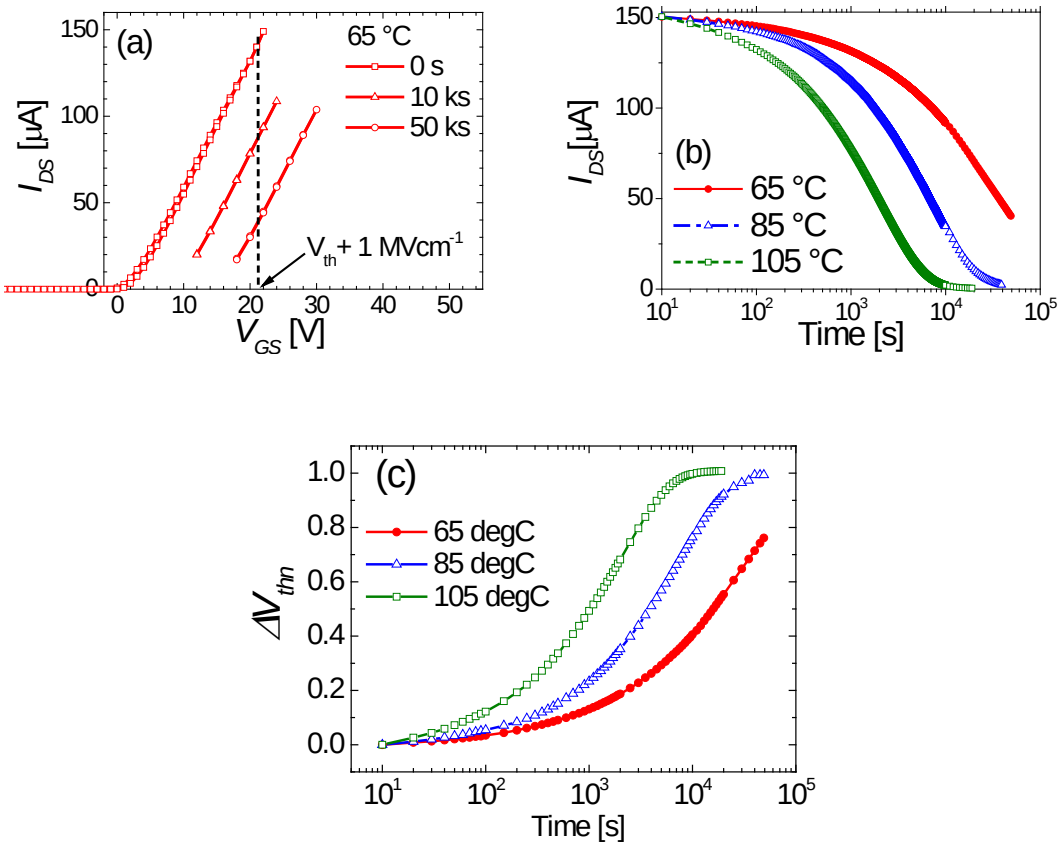

Figure 2. (a) Linear I_{DS} as a function of V_{GS} measured at a PBS temperature of 65 °C at 0, 10,000 and 50,000 s, (b) the I_{DS} and (c) the ΔV_{thn} as a function of stressing time at 65, 85 and 105 °C. An a-ZTO TFT with a channel width and length of 1000 μm and 20 μm ($W/L = 50$) is used.

Using the thermalization energy analysis in equation [1], the ΔV_{thn} as a function time can be converted to the ΔV_{thn} as a function of thermalisation energy. Figure 3a shows that the ΔV_{thn} vs. E_{th} curves for the three temperatures overlap optimally at an attempt-to-escape frequency, at $\nu = 10^7$ s^{-1}. Figure 3b shows the corresponding derivative. The data in Figure 3a is fitted to a stretched hyperbola (20)

$$\Delta V_n(t) = 1 - \left[\exp\left(\frac{E_{th} - E_A}{k_B T_0} \right) + 1 \right]^{-2} \qquad [3]$$

where E_A and k_BT_0 represent a measure of the characteristic energy barrier for the process and the width of the energy distribution respectively. The stretched hyperbola can be differentiated to give the curve in Figure 3b. The maximum energy barrier, E_{max} is obtained using the relation

$$E_{\max} = E_A - k_B T_0 \ln 2 \qquad [4]$$

E_{max} ~ 0.76 eV and k_BT_0 ~ 100 meV are extracted for the a-ZTO TFT.

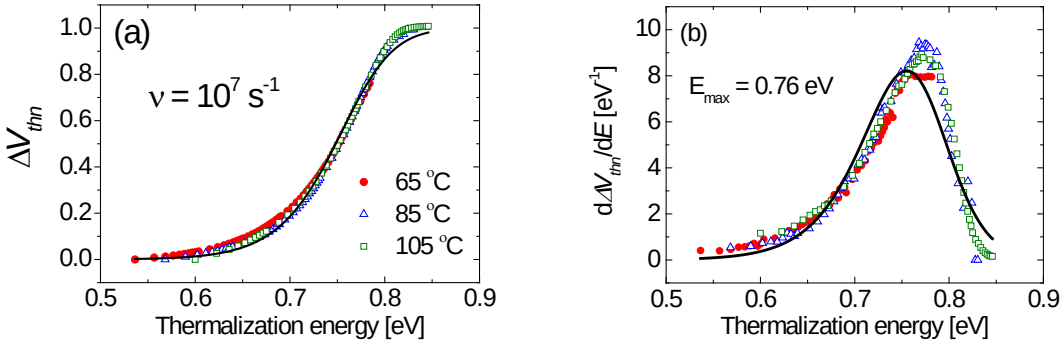

Figure 3. (a) The normalized threshold voltage shifts and (b) the corresponding derivatives as a function of thermalization energy at temperatures of 65, 85 and 105 °C for a-ZTO TFTs. The optimal overlap is obtained with an attempt-to-escape frequency, $\nu = 10^7$ s^{-1}. The solid lines in (a) and (b) are a fit based on a stretched hyperbola and its derivative respectively.

Table 1 compares the parameters extracted from the thermalization energy analysis for various oxides TFTs and thin film Si TFTs. We have previously reported that the E_{max} and ν extracted for a-IGZO under PBS is in the same range as those under NBIS, suggesting the same physical process is responsible for both PBS and NBIS (23). In this report, the E_{max} and ν extracted for a-ZTO under PBS is also very similar to that of a-IGZO, suggesting the same physical process is occurring in a-ZTO as in a-IGZO. On the other hand, as shown in Table 1 the E_{max} and ν of a-Si:H and μc-Si TFT are ~ 1 eV and 10^{10} s^{-1} respectively, which are very different from those of oxide TFTs.

The beauty of the thermalization energy analysis lies in the fact that the approach is agnostic to the mechanism by which the threshold voltage shift is occurring. Table 1 shows that the parameters extracted are very similar within the same material group. Moreover, the only fitting parameter, ν, indicates the distance of the localization of

carriers in the band tail states. In a-Si:H, ν is 10^3 smaller than the typical phonon frequency which is ~ 10^{13} s^{-1}. This implies ~ 10^3 increase in the volume of space occupied by an electron compared with one localized completely within a bond, and hence that the electrons in the band tail states are localized within ~ 2 nm of the potential defect creation site in a-Si:H (22). In the same way, the localization of carriers in the band tail states are estimated to be ~ 20 to 40 nm in a-IGZO and ~ 20 nm in a-ZTO based on the attempt-to-escape frequencies. This physical interpretation is another advantage of the thermalization energy analysis.

The microscopic mechanism responsible for the instability in a-Si:H is attributed to the creation of dangling bond defects and their hydrogen stabilization by Powell *et al.* (26). This process is described by the reversible reaction

$$\mathrm{SiHHSi} + \mathrm{Si} - \mathrm{Si} \Leftrightarrow 2\mathrm{SiH(db)Si} \qquad [5]$$

where SiHHSi is two Si—H bonds in close proximity, Si—Si is a weak silicon bond and 2SiH(db)Si is a single Si—H bond and a silicon dangling bond in close proximity. The above reaction is also depicted in Figure 4, showing the H_2^* configuration in crystalline Si taking the form of a SiHHSi complex. Under a non-equilibrium condition such as an applied bias, the breaking of a weak Si—Si bond and a local rearrangement of the hydrogen atoms produces two SiH(db)Si states as shown in Figure 4b. The transitions between the two states needed to overcome the energy barrier is the E_{max} and the attempts made to overcome the barrier, ν, which are extracted experimentally. This mechanism is applicable to both a-Si:H and μc-Si:H TFTs as indicated by similar E_{max} and ν in Table 1.

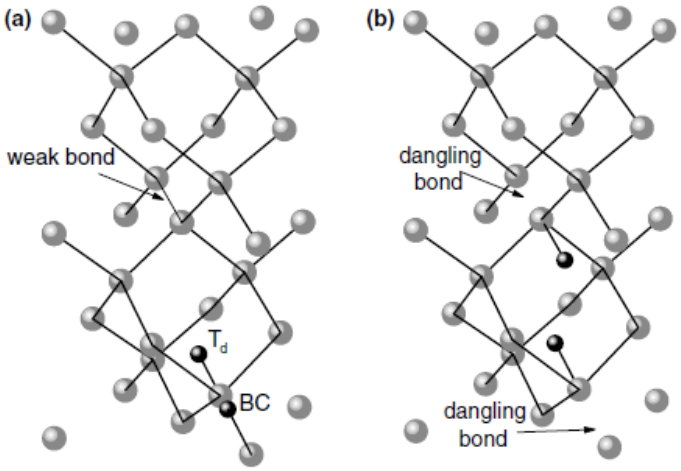

Figure 4. Schematics of (a) H_2^* complex showing hydrogen atoms (in black) in both the Bond Centered (BC) and tetrahedral (T_d) positions; (b) the corresponding dangling bond defect states, after (27). Reprinted from Journal of Non-Crystalline Solids, Vol. 352, A. J. Flewitt, S. Lin, W. I. Milne, R. B. Wehrspohn, M. J. Powell, Characterization of defect removal in hydrogenated and deuterated amorphous silicon thin film transistors, Pages 1700–1703, (2006), with permission from Elsevier.

It is generally accepted that the origin of instability in AOS TFTs are the oxygen vacancies, which have been directly measured using hard x-ray photoelectron spectroscopy by the Nomura group (28, 29). Recently, Flewitt and Powell proposed the defect pool model of defect states in AOS and that the thermally equilibrated distribution

of states is achieved through oxygen vacancy migration (19). This is analogous to the defect pool for amorphous silicon. However, unlike the defect creation model in amorphous silicon, a defect conversion between the charged (V_O^{2+}) and uncharged (V_O) oxygen vacancies is proposed (19). Under a PBS, the field-induced electrons encourage the conversion of charged V_O^{2+} states in the upper part of the band gap to uncharged V_O states in the lower part of the band gap, with the energy barrier to the process being caused by the need for an oxygen 2– ion to migrate through an intermediate interstitial state. The number of defect states in lower part of the band gap (called D_e states) is increased while those in the upper part of the band gap (called D_h states) is reduced by the same amount. The process may be summarized as

$$D_h^{2+} + [O(—M)_n + 2e] \rightarrow D_h^{2+} + O_i^{2-} + D_e \rightarrow O(—M)_n + D_e \qquad [6]$$

where $O(—M)_n$ is an *n*-coordinated oxygen atom neighboring the D_h site, $[O(—M)_n + 2e]$ represents electron localization close to such a site, and O_i^{2-} is an oxygen ion migrating through an interstitial (barrier) site. The process is depicted in Figure 5.

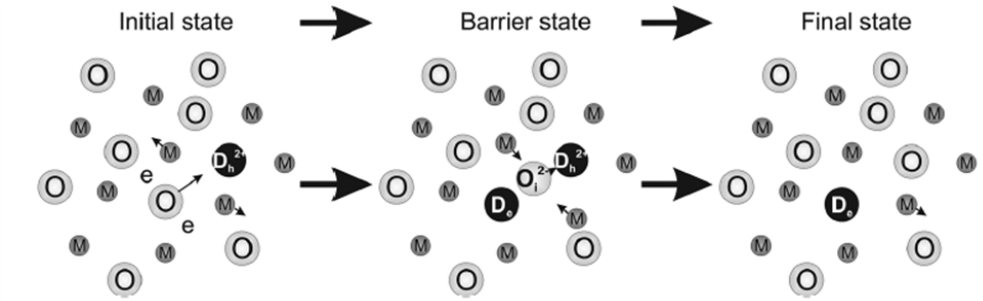

Figure 5. Schematics of defect conversion process of PBS. Shaded circles with an M and O represent metal and oxygen atoms, respectively. Solid black circles are the oxygen vacancy states. When an oxygen atom is in an interstitial state, it is represented by O_i and any charge state is indicated. Arrows indicate that some movement will be taking place. Initial, final, and the barrier states are all shown. It is the energy barrier state (i.e., the oxygen vacancy migration energy) that defines the energy barrier for the process and the resulting metastability, after (19). Reprinted from Journal of Applied Physics 115, 134501 (2014) with the permission of AIP Publishing.

The oxygen vacancy migration model is consistent with the thermaliation energy analysis of PBS. There is a clear barrier to defect conversion in the formation of the O_i site, and the energy extracted is consistent with theoretical calculations. Also, as carriers are only weakly localized around these defect migration sites, the attempt-to-escape frequency is reduced from the phonon frequency to ~10^7 s^{-1}, as extracted. Moreover, the oxygen vacancy migration model is consistent with the V_{th} shift observed under PBS in a-ZTO and a-IGZO TFTs. Under a PBS, field induced electrons are localized on D_h states that encourage the reaction in equation [3]. As a result, more D_e states will be formed and this will pull the Fermi level lower in the band gap when the gate bias is removed, leading to an increased V_{th} as observed experimentally (19). This oxygen vacancy migration model also ties in well with the evidence of movement of H and O atoms in a-IGZO reported by Nomura *et al.* (30) and the interplay between the oxygen interstitials and hydrogen, which is linked to the NBIS characteristics reported by Robertson and Guo recently (31).

TABLE I. Comparison of the attempt-to-escape frequency, ν, and the peak energy for defect conversion, E_{max}, and distribution, k_BT_0, for various oxide TFTs and thin film silicon TFTs under PBS or NBIS.

Type of TFT	Channel	Type of Stress	ν [s^{-1}]	E_{max} [eV]	k_BT_0 [meV]	Ref.
Bottom gate	a-ZTO	PBS	10^7	0.76	100	This work
Bottom gate	a-IGZO	PBS	10^7	0.75	100	Niang (23)
		NBIS	10^6–10^7	0.65–0.75	250	Flewitt (19)
Bottom gate	a-Si:H	PBS	10^{10}	0.85–1.00	55–88	Deane (20)
Bottom gate	μc-Si:H	PBS	10^{10}	1.07	68	Wehrspohn (22)

Finally, it should be noted that the back channel of a-ZTO is not passivated whereas that of a-IGZO in ref. (23) is passivated with SU-8 by spin coating. In spite of that, the instability parameters in Table 1 are very similar. This agrees with the report that ZTOs have a higher tolerance to chemicals and ambient conditions than zinc oxide (32). Nonetheless, how the stability of non-passivated a-ZTO TFTs will be affected by environment as they age need to be monitored.

Conclusions

Stability under positive gate bias stressing of a-ZTO TFTs has been investigated, and a thermalization energy analysis is applied. A maximum energy barrier to defect migration of 0.76 eV and the attempt-to-escape frequency of 10^7 s^{-1} are extracted. A carrier localization length around the defect migration site ~ 20 nm is estimated. These values are similar to those extracted previously for a-IGZO TFTs, indicating that the same oxygen vacancy migration process for threshold voltage instability is responsible. This is different from the defect creation model proposed for a-Si:H TFTs.

Acknowledgments

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